Abstract of the Disclosure

A DSP (Digital Signal Processing) architecture with a wide memory bandwidth and a memory mapping method thereof. The DSP architecture includes: a first communication port; first, second, and third memory devices, which are connected with the first communication port and are arranged in a first row direction of the DSP architecture; a fourth memory device, a calculation element, and a fifth memory device, which are arranged in a second row direction below a first row direction of the DSP architecture; and sixth, seventh, and eighth memory devices, which are connected with the first communication port and arranged in a third row direction of the DSP architecture, wherein the calculation element is connected with the first through the eight memory devices. In the DSP architecture, the calculation element and the first through the eighth memory devices form one arrangement unit, wherein the calculation element is disposed in the center of the arrangement unit, the first through the eighth memory devices are connected to the calculation element, and a plurality of arrangement units are arranged in row directions and column directions of the DSP architecture. Therefore, since a wide data bandwidth is provided between the calculation element of the DSP architecture and the memory devices, it is possible to reduce memory access times when data is processed, and accordingly, to process data with a high data rate, such as a moving image with a high resolution.